We claim:

1. A method for forming a doped region in a semiconductor substrate, comprising:

providing a semiconductor;

forming a patterned photoresist layer comprising at least one opening on said semiconductor;

implanting a first species into said semiconductor through said opening;

performing a hard bake on said patterned photoresist layer; and

implanting a second species into said semiconductor through said opening.

2. The method of claim 1 wherein said semiconductor comprises an epitaxial layer.

3. The method of claim 1 wherein said hard bake comprises heating said patterned photoresist layer to temperatures between 75°C and 200°C.

4. The method of claim 3 wherein said first dopant species comprises a light mass implant specie.

5. The method of claim 4 wherein said second dopant species comprises a heavy mass implant specie.

6. A method for forming a double diffused region, comprising:

providing a semiconductor;

forming a patterned photoresist layer over said semiconductor wherein said patterned photoresist layer comprises at least one opening;

implanting a boron species into a region of said semiconductor through said opening;

performing a hard bake process on said patterned photoresist layer;

implanting an arsenic species into said region of said semiconductor through said opening; and

performing at least one thermal annealing cycle on said semiconductor.

7. The method of claim 6 wherein said thermal annealing cycle occurs at temperatures between 800°C and 1200°C.

8. A method for forming a LDMOS transistor, comprising:

forming an epitaxial layer on a semiconductor substrate;

forming a deep n-well region in said epitaxial layer;

forming a patterned photoresist layer over said deep n-well region wherein said patterned photoresist layer comprises at least one opening;

implanting a boron species into said deep n-well through said opening;

performing a hard bake process on said patterned photoresist layer;

implanting an arsenic species into said deep n-well through said opening;

forming LOCOS isolation structures in said deep n-well region; and

forming a gate dielectric layer on said deep n-well region.

9. The method of claim 8 wherein said hard bake process comprises heating said patterned photoresist layer to temperatures between 75°C and 200°C.

10. The method of claim 9 wherein forming said LOCOS isolation structures comprises performing thermal oxidation processes at temperatures greater than 800°C.